Attorney Docket No.: Q76416

Application No.: 10/612,929

## REMARKS

Claims 19-36 are all the claims pending in the application.

## I. Claim Objections

Claims 25-30 are objected to because of informalities. Applicant hereby amends claims 25-30, without narrowing, to cure the informalities and overcome the objection.

## II. Claim Rejections under 35 U.S.C. § 102(b)

Claims 19-36 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,751,932 to Horst et al. (hereinafter "Horst"). Applicant respectfully traverses this rejection and respectfully requests the Examiner to reconsider this rejection at least in light of the comments which follow.

Only claim 19 is independent. Turning first to claim 19, the Examiner alleges that Horst discloses "said first controller writes data to said first main-memory and said second submemory according to a first write request of said first processor, and at the substantially same time, said second controller writes data to said second main-memory and said first sub-memory according to a second write request of said second processor," as recited, *inter alia*, in claim 19. Applicant respectfully disagrees.

Instead of writing data to a first main-<u>memory</u>, a second main-<u>memory</u>, a first sub-<u>memory</u>, and a second sub-<u>memory</u>, Horst discloses that data is written by each CPU, one bit at a time, to output <u>registers</u>, which are communicated via bus lines to remote input <u>registers</u>, which are read by each CPU (*see* col. 73, lines 3-22 of Horst). A person of ordinary skill in the art would clearly understand that <u>registers</u> are necessarily different from the main-<u>memory</u> and subAMENDMENT UNDER 37 C.F.R. § 1.116 Attorney Docket No.: Q76416

Application No.: 10/612,929

memory recited, *inter alia*, in claim 1 because, unlike main-memory and sub-memory, registers store only very small amounts of data.

Furthermore, Horst discloses that, if asymmetric variables were simply read by each of the two duplexed CPUs then written to the memory, the contents of each CPU's memory would thereby differ by at least the value read by each (*see* col. 71, lines 56-63 of Horst).

Consequently, Horst discloses that the asymmetric variables are written to registers and thus communicated to both CPUs without writing the asymmetric variables to the memory (*see* col. 71, line 64-col. 72, line 33 of Horst). Therefore, it is necessarily implicit in Horst's disclosure that registers are not the same as memory. Accordingly, Horst does not disclose writing data to a first main-memory, a second main-memory, a first sub-memory, and a second sub-memory.

The Examiner further alleges that Horst discloses "wherein said first and second write requests are associated with the same data," as recited, *inter alia*, in claim 19. Applicant respectfully disagrees.

Even if, *arguendo*, Horst discloses the first and second write requests, which Applicant respectfully submits Horst does not disclose, instead of the first and second write requests being associated with the same data, Horst discloses that the first and second write requests are associated with different, <u>asymmetric</u>, data (*see* col. 71, line 45-col. 72, line 33 and col. 72, line 61-col. 73, line 22 of Horst).

It is noted that claim 19 includes the feature that the first controller writes data according to a first write request of the first processor, and the second controller writes data according to a second write request of the second processor, as discussed above. Horst discloses that an example of an asymmetric variable is a serial number that is different for each CPU (*see* col. 71, lines 48-55). In this example, the write request of the first CPU (first write request) would be

Attorney Docket No.: Q76416 AMENDMENT UNDER 37 C.F.R. § 1.116

Application No.: 10/612,929

associated with the first CPU's serial number, and the write request of the second CPU (second

write request) would be associated with the second CPU's serial number, which is different (see

col. 71, line 45-col. 72, line 33 and col. 72, line 61-col. 73, line 22 of Horst). Accordingly, Horst

does not disclose that the first and second write requests are associated with the same data.

For at least the reasons discussed above, Applicant respectfully submits that claim 19 is

patentable over Horst. Applicant respectfully submits that claims 20-36 are patentable over

Horst at least by virtue of their dependency on claim 19.

III. Conclusion

In view of the above, reconsideration and allowance of this application are now believed

to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is

kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue

Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any

overpayments to said Deposit Account.

Respectfully submitted,

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9